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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,227	02/14/2002	Takashi Miida		6199

7590 08/18/2003

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EXAMINER
YAM, STEPHEN K

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 08/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,227	MIIDA, TAKASHI	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 17* is/are allowed.

6)☒ Claim(s) *4-10 and 12-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action is in response to Amendments and remarks filed on May 27, 2003. Claims 4-17 are currently pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsay et al. US Patent No. 6,529,237 in view of Kozlowski et al. US Patent No. 5,892,540.

Regarding Claims 4-6, Tsay et al. teach (see Fig. 1 and 2) a solid-state imaging device in which an optical signal is converted into an electric signal, the electric signal is converted into a digital signal (D_{OUT}) (see Fig. 1), and the digital signal is outputted, comprising a plurality of photoelectric conversion devices (10), for converting the optical signal into the electric signal and outputting a signal voltage, a variable gain amplifier (14), including an input terminal (32) of the variable gain amplifier for sequentially inputting a first signal voltage (118) (see Fig. 3) obtained from a corresponding photoelectric conversion device by converting an optical signal into an electric signal (see Col. 4, lines 31-35) and a second signal voltage (112) (see Fig. 3) obtained by initializing the corresponding photoelectric conversion device (see Col. 3, lines 63-66 and Col. 4, lines 27-31), an output terminal, an output terminal (V_p) of the variable gain amplifier for outputting a difference signal between the first signal voltage and the second signal

voltage (see Col. 4, lines 5-7), an operational amplifier (68) having a positive input terminal for inputting a reference voltage, a negative input terminal connected through a signal path to the input terminal of the variable gain amplifier, and an output terminal connected to the output terminal of the variable gain amplifier, an input capacitor (46) having a variable capacitance provided in the signal path extending from the input terminal of the variable gain amplifier to the negative input terminal of the operational amplifier, the input capacitor having one end connected through the signal path to the input terminal of the variable gain amplifier and having the other end connected through the signal path to the negative input terminal of the operational amplifier, a feedback capacitor provided between the negative input terminal and the output terminal of the operational amplifier, a first switch device (38) for connecting or disconnecting the signal path, a second switch device (54) for connecting or disconnecting an input of the reference voltage to the one end of the input capacitor, and a third switch device (96) for connecting or disconnecting the negative input terminal and the output terminal of the operational amplifier, and an analog/digital conversion circuit (18) converting the difference signal outputted from the variable gain amplifier to a digital signal (D_{OUT}). Regarding Claim 5, Tsay et al. teach (see Fig. 5) the input capacitor having variable capacitance and comprising a plurality of capacitors (130) and a plurality of switch devices, wherein one or more capacitors necessary for setting the capacitance of the input capacitor can be selected from the plurality of capacitors by one or more switch devices among said plurality of switch devices. Tsay et al. do not teach the photoelectric conversion devices arrayed in rows and columns, a variable gain amplifier provided for each column, and the feedback capacitor (instead of the input capacitor) having a variable capacitance. Kozlowski et al. teach (see Fig. 1) an imager with a plurality of

photoelectric conversion devices (12) arrayed in rows and columns (see Col. 5, lines 43-55) leading to an amplifier (24) for every column (see Col. 5, lines 21-23 and 49-50) for sequentially inputting (see Col. 6, lines 44-48) a first and second signal voltage and generating a difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42) and a analog/digital conversion circuit (see Col. 4, lines 5-7) for converting the output of the amplifier to a digital signal. In addition, it is well known in the art to interchange the input and feedback capacitors with variable-capacitance abilities, as changing the ratio between the input and feedback capacitance affects the gain, so changing either the input or feedback capacitance will provide a desired change in the amplifier gain. It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the photoelectric conversion devices in rows and columns with a variable-gain amplifier for every column as taught by Kozlowski et al. and to provide adjustable capacitance in the feedback capacitor instead of the input capacitor in the device of Tsay et al., to provide more adjustment for the gain characteristics for each column of a two-dimensional photodetection array and vary the filter characteristics of the amplifier as desired for a particular signal frequency.

Regarding Claim 7, Tsay et al. in view of Kozlowski et al. teach the device as taught in Claim 4, according to the appropriate paragraph above. Tsay et al. also teach each of the photoelectric conversion devices comprising a photodetector and outputting a first and second signal voltage (see Col. 1, lines 49-52). Kozlowski et al. also teach (see Fig. 1) each of the photoelectric conversion devices (12) comprising a photodetector (14) and a field effect transistor (16) provided adjacently to the photodetector to output a first and second signal voltage for correlated doubling sampling. Tsay et al. do not teach a field effect transistor as having an

insulated gate with a heavily doped buried layer around a source region under a channel region below a gate electrode. It is well known in the art to construct a photodetector using a heavily doped source layer to provide specific current-channel characteristics and use a field effect transistor with a gate electrode above the source and drain regions to control the current flow. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a heavily doped source layer and a field effect transistor with a gate electrode in the device of Tsay et al. in view of Kozlowski et al., to provide specific current and voltage characteristics for efficiently outputting the electrical signal converted by the photodetector.

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsay et al. in view of Satoh US Patent No. 6,342,694.

Tsay et al. teach (see Fig. 1 and 2) an optical signal reading method comprising irradiating a photoelectric conversion device (10) with an optical signal, outputting a first signal voltage (118) (see Fig. 3) obtained by converting the optical signal into an electric signal, converting (see Col. 6, lines 44-46) the first signal voltage into charges and storing the charges, outputting (see Col. 6, lines 45-48) a second signal charge at an initialization (reset) of the photoelectric conversion device same as that obtaining the first signal voltage (see Col. 4, lines 16-35), converting (see Col. 6, lines 49-51) the second signal voltage into charges (in the capacitor), generating a difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42) between the first signal voltage and the second signal voltage, and converting (see Col. 4, lines 2-7) the difference signal into a digital signal. Kozlowski et al. also teach a gain-adjustable amplifier (22) and altering the gain of the amplifier for each frame (see

Col. 3, lines 17-20). Tsay et al. do not teach adjusting the gain according to the difference signal and outputting an adjusted difference signal. Satoh teaches (see Fig. 9) an amplifier (3) for a photodiode (1) wherein the gain of the amplifier is adjusted (see Col. 5, lines 33-42) based on the amplitude of a difference signal (out of (14)) between a first (V_{OUT} stored in (10)) and second signal (V_{REF} stored in (12)), and hence outputting an adjusted output (see Col. 5, lines 41-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the gain of the amplifier according to the difference signal as taught by Satoh in the method of Tsay et al., to provide real-time adjustment of a dynamic range to enable linear amplifier gain for accurate amplification.

4. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsay et al. in view of Satoh, further in view of Kozlowski et al.

Regarding Claim 9, Tsay et al. in view of Satoh teach the method in Claim 8, according to the appropriate paragraph above. Tsay et al. also teach a plurality of photoelectric conversion devices (see Col. 1, lines 48-52). Tsay et al. do not teach a plurality of photoelectric conversion devices arrayed in rows and columns and the difference signal having the output level adjusted is outputted for each column. Kozlowski et al. teach (see Fig. 1) an imager with a plurality of photoelectric conversion devices (12) arrayed in rows and columns (see Col. 5, lines 43-55) leading to an amplifier (24) for every column (see Col. 5, lines 21-23 and 49-50) for sequentially inputting (see Col. 6, lines 44-48) a first and second signal voltage and outputting a difference signal (inherent within a correlated-double-sampling process) (see Col. 6, lines 40-42) for each column and a analog/digital conversion circuit (see Col. 4, lines 5-7) for converting the output of

the amplifier to a digital signal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the photoelectric conversion devices in rows and columns with a variable-gain amplifier for every column and output a difference signal for every column as taught by Kozlowski et al. in the method of Tsay et al. in view of Satoh, to provide more adjustment for the gain characteristics for each column of a two-dimensional photodetection array.

Regarding Claim 10, Tsay et al. in view of Satoh and Kozlowski et al. teach the method in Claim 8, according to the appropriate paragraph above. Tsay et al. also teach each of the photoelectric conversion devices comprising a photodetector and outputting a first and second signal voltage (see Col. 1, lines 49-52). Kozlowski et al. also teach (see Fig. 1) each of the photoelectric conversion devices (12) comprising a photodetector (14) and a field effect transistor (16) provided adjacently to the photodetector to output a first and second signal voltage for correlated doubling sampling. Tsay et al. do not teach a field effect transistor having an insulated gate with a heavily doped buried layer around a source region under a channel region below a gate electrode. It is well known in the art to construct a photodetector using a heavily doped source layer to provide specific current-channel characteristics and use a field effect transistor with a gate electrode above the source and drain regions to control the current flow. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a heavily doped source layer and a field effect transistor with a gate electrode in the device of Tsay et al. in view of Satoh and Kozlowski et al., to provide specific current and voltage characteristics for efficiently outputting the electrical signal converted by the photodetector.

5. Claims 12 and 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsay et al. in view of Yonemoto US Patent No. 5,717,458.

Tsay et al. teach (see Figs. 1 and 2) a solid-state imaging device and method comprising a plurality (10) (see Col. 1, lines 48-52) of photoelectric conversion devices for converting an optical signal into an electric signal and outputting the electric signal, an amplifier (14) for sequentially inputting a first signal voltage (118) (see Fig. 3) and a second signal voltage (112) (see Fig. 3) obtained by initializing the photoelectric conversion device (see Col. 3, lines 63-66 and Col. 4, lines 27-31), converting the first and second signal voltage into charges (), and outputting a difference signal (see Col. 4, lines 5-7) between the first and second signal voltage, and a video signal output terminal (D_{out}) for outputting the difference signal as a video signal corresponding to the optical signal (see Col. 1, lines 18-20). Tsay et al. do not teach the photoelectric conversion devices arrayed in rows and columns, an amplifier for each of the columns, and a switching means provided between respective input sides of the amplifiers of at least two columns for mixing the difference signals of at least two columns. Yonemoto teaches (see Fig. 21) a solid-state imaging device with a plurality of photoelectric conversion devices (1) arrayed in rows and columns with a switching means (43) provided between respective input sides of at least two columns for mixing the difference signals of at least two rows (see Col. 17, lines 50-57)- a row and column are equivalent as rotating the imager physically by 90° changes a row to a column and vice versa. In addition, it is well known in the art to use an amplifier for every column in a two-dimensional photodetection array. It would have been obvious to one of ordinary skill in the art at the time the invention was made to array the photoelectric conversion devices in rows and columns and provide a switching means between rows or columns as taught

by Yonemoto along with providing an amplifier for each column in the device of Tsay et al., to provide imaging and to lower the required photodetection time to provide higher video speed, and provide more adjustment for the individual gain characteristics for each column of a two-dimensional photodetection array.

6. Claims 13, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsay et al. in view of Yonemoto, further in view of Satoh.

Regarding Claim 13, Tsay et al. in view of Yonemoto teach the device in Claim 12, according to the appropriate paragraph above. Tsay et al. also teach the amplifier as a variable gain amplifier (see Fig. 5) in which the first and second signal voltage are sequentially inputted (see Col. 4, lines 16-36), converted (see Col. 6, lines 44-46) to charges, a difference voltage is generated (see Col. 4, lines 9-14). a gain is adjusted according to an amplitude of the difference signal, and a difference signal adjusted in a output level is outputted. Tsay et al. do not teach adjusting the gain according to the difference signal and outputting an adjusted difference signal. Satoh teaches (see Fig. 9) an amplifier (3) for a photodiode (1) wherein the gain of the amplifier is adjusted (see Col. 5, lines 33-42) based on the amplitude of a difference signal (out of (14)) between a first (V_{OUT} stored in (10)) and second signal (V_{REF} stored in (12)), and hence outputting an adjusted output (see Col. 5, lines 41-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the gain of the amplifier according to the difference signal as taught by Satoh in the method of Tsay et al. in view of Yonemoto, to provide real-time adjustment of a dynamic range to enable linear amplifier gain for accurate amplification.

Regarding Claims 14 and 16, Tsay et al. in view of Yonemoto and Satoh teach the device and method in Claims 13 and 15, according to the appropriate paragraph above. Tsay et al. also teach each of the photoelectric conversion devices comprising a photodetector and outputting a first and second signal voltage (see Col. 1, lines 49-52). Tsay et al. do not teach a field effect transistor having an insulated gate with a heavily doped buried layer around a source region under a channel region below a gate electrode. It is well known in the art to construct a photodetector using a heavily doped source layer to provide specific current-channel characteristics and use a field effect transistor with a gate electrode above the source and drain regions to control the current flow. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a heavily doped source layer and a field effect transistor with a gate electrode in the device of Tsay et al. in view of Satoh and Kozlowski et al., to provide specific current and voltage characteristics for efficiently outputting the electrical signal converted by the photodetector.

Allowable Subject Matter

7. Claims 11 and 17 are allowed over the prior art of record.

8. The following is a statement of reasons for the indication of allowable subject matter: Regarding Claims 11 and 17, the amplifier as claimed, specifically in combination with the method of connecting and disconnecting the appropriate switches to store charges from the first signal voltage in the input capacitor, transfer it to the feedback capacitor, read a second signal voltage, generate a difference signal between the first and the second signals, and adjust the gain

of the amplifier according to the difference signal, is not disclosed or made obvious by the prior art of record.

Response to Arguments

9. Applicant's arguments with respect to claims 4-10 and 12-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (703)306-3441. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (703)308-4852. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7724 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

SY

SY
August 4, 2003

DAVID PORTA
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